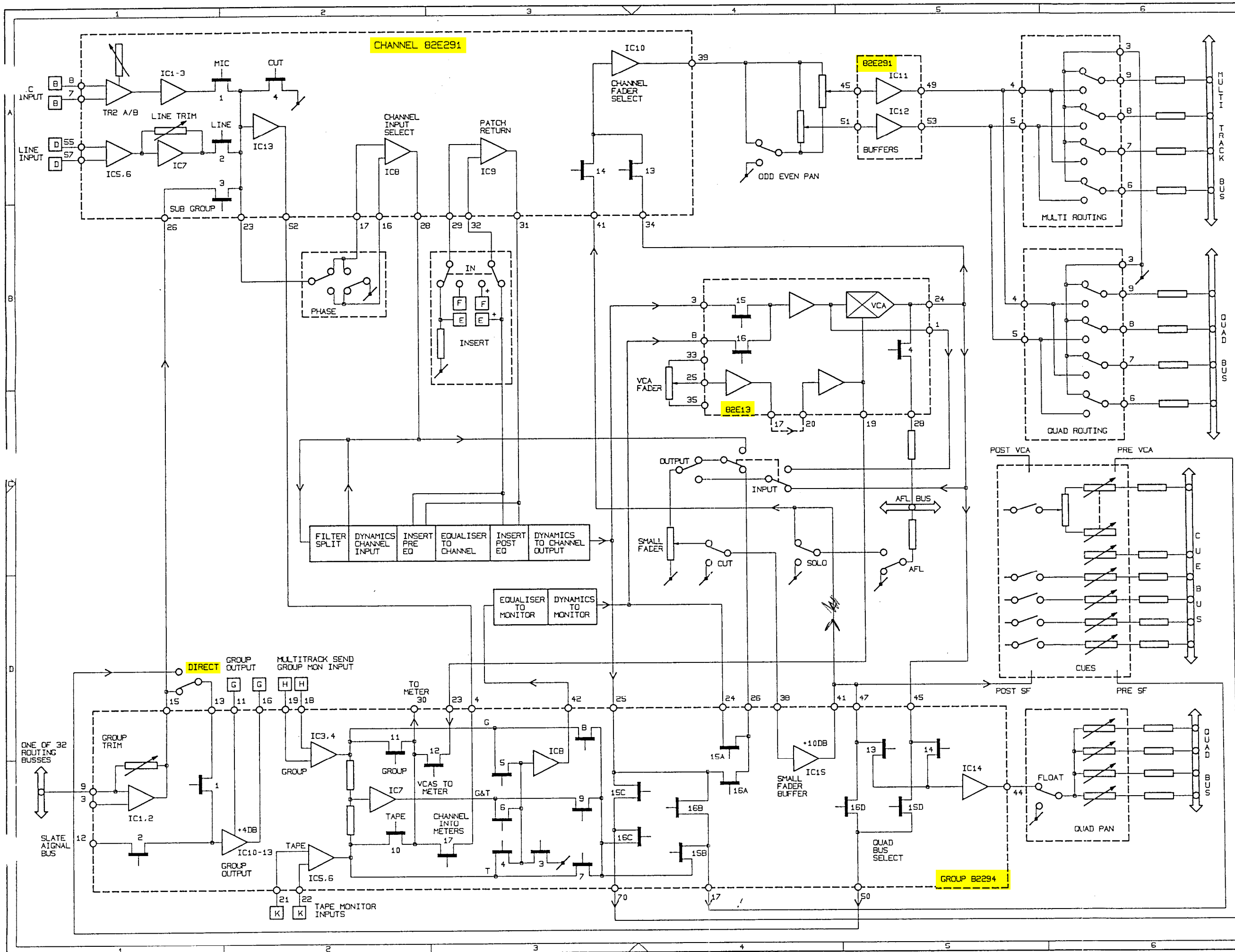




| COPYRIGHT © SSL ALL RIGHTS RESERVED. THIS DOCUMENT MAY NOT BE REPRODUCED IN ANY FORM WITHOUT THE WRITTEN PERMISSION OF SOLID STATE LOGIC. |       |        |                                                                          |
|-------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|--------------------------------------------------------------------------|
| REV                                                                                                                                       | ISSUE | DATE   | DETAILS                                                                  |
| A                                                                                                                                         | 25    | JAN 88 | NEW DRAWING DTG STEFF                                                    |
| B                                                                                                                                         | 28    | FEB 89 | 82E01 DELETED 82E2S1 INSERTED STEFF                                      |
| C                                                                                                                                         | 11    | SEP 92 | DCR/670 REF CORRECTED FROM IC10 TO IC12 BETWEEN 82E291 PINS S1 AND S3 MM |
| SHEET 1 OF 1                                                                                                                              |       |        |                                                                          |
| REF: T611GB A2                                                                                                                            |       |        |                                                                          |
| E TITLE 611G SERIES I/O MODULE BLOCK SCHEMATIC                                                                                            |       |        |                                                                          |
| DRG. NO. T0611G.41                                                                                                                        |       |        |                                                                          |
| Solid State Logic                                                                                                                         |       |        |                                                                          |